REMARKS/ARGUMENTS

Applicants amend claims 9 and 21 to remove an extraneous instance of "at".

1. Claims 1-25 and 29-40 are Patentable Over the Cited Art

The Examiner rejected claims 1-25 and 29-40 as obvious (35 U.S.C. §103) over Hassan (U.S. Patent No. 7,280,542) in view of Verplanken (U.S. Patent No. 6,038,592). Applicants traverse for the following reasons.

Amended claims 1, 13, and 29 require receiving a multicast packet to transmit to destination addresses; writing a payload of the multicast packet to at least one packet entry in a packet memory; generating headers for the destination addresses; generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and generating, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor, and wherein a plurality of the indicators generated for a plurality of the destination addresses indicate a same at least one descriptor identifying at least one packet entry to be provided for the plurality of the destination addresses for which the plurality of indicators are generated.

The added requirement that a plurality of the indicators generated for a plurality of the destination addresses indicate a same at least one descriptor identifying at least one packet entry to be provided for the plurality of the destination addresses for which the plurality of indicators are generated is disclosed in at least FIGs. 2a, 2b,and 3 and paras. 19-23 of the filed Specification.

The Examiner cited col. 11, lines 44-48 and FIG. 5 of Hassan as teaching the claim requirement of generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses. (OA2, pg. 3) The Examiner cited the pointers 514B in FIG. 5 as teaching the descriptor addressing a packet entry in packet memory including the payload to transmit. The pointers 514B address the cell memory locations 516-1 to516-K in FIG. 5.

The Examiner further cited co. 11, lines 25-28 and 44-48 of Hassan as teaching the claim requirement of generating, for each destination address, at least one indicator including

information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor. (OA2, pg. 2). However, a review of this cited Hassan does not teach generating for each destination address an indicator that has information on at least one descriptor to provide for the destination address the payload, where a plurality of the indicators generated for a plurality of the destination addresses indicate a same at least one descriptor identifying at least one packet entry to be provided for the plurality of the destination addresses for which the plurality of indicators are generated. A review reveals that the Examiner has not cited where Hassan teaches generating for each destination address a descriptor that has information on one of the pointers 514B to provide the payload for the destination address, or that a plurality of the indicators generated for a plurality of the destination addresses indicate a same at least one descriptor identifying at least one packet entry to be provided for the plurality of the destination addresses for which the plurality of indicators are generated.

Hassan concerns point-to-multipoint connections, which is a multicast. For multicasting, a single source of traffic (the root) emits cells or packets to a number of destinations (leaves) that receive the replicated traffic. A leaf flow must not interfere with the transmission to other leaves. (Hassan, col. 2, lines 51-64) Reference numerals 408 refer to N leaf flows, where each leaf flow is initialized with an index pointer to pointer memory. Reference numerals 410-1 to 410-N refer to N leaf index pointer values associated with N leaf flows. (Hassan col. 9, lines 28-40).

The cited col. 11, lines 44-48 mention that a linked buffer 510 includes an index relating to a leaf and root flow index values and a pointer containing pointers to the cell memory locations. The root cells are stored or written too using the root index as they are enqueued for MC (multicast) service. The cell memory effects MC scheduling operations. The cited col. 11 mentions that for the MC scheduling operations, leaf index values correspond to N leaf flows associated with a root flow. A linked buffer has an index portion relating to the leaf and root flow index values and a pointer location portion pointing to the cell memory locations, having cells enqueued for an MC service. Hassan mentions that in the MC flow arrangement, a root flow is transmitted to a plurality of egress interfaces using leaf flows, and that a scheduler implements the MC scheduling activity. (Hassan, col. 9, lines 13-25)

Although the cited Hassan discusses a multicast (MC) flow, the cited Hassan does not teach the claim requirement that an indicator is generated for each destination address including information on at least one descriptor that addresses at least one packet entry including the payload for the destination address. Further, there is no teaching of the added claim requirement that a plurality of the indicators generated for a plurality of the destination addresses indicate a same at least one descriptor identifying at least one packet entry to be provided for the plurality of the destination addresses for which the plurality of indicators are generated.

The Examiner has not cited shown where Hassan teaches that for each destination address, there is an indicator having information on a pointer 514B, which the Examiner likens to the descriptors. Instead, the cited Hassan mentions that leaf flows 410 include a pointer or index to the pointers 514B. The Examiner has not shown where Hassan teaches that the cited leaf flows have pointers 514B address identifying the same entries in the cell memory 506 that have payload for a multicast packet. Instead, the cited FIG. 5 shows that each pointer points to a different entry in the cell memory. The cited FIG. 5 does not teach multiple indicators having the same descriptors identifying the same payload locations in the memory to include for multiple destination address.

The Examiner cited col. 7, lines 1-8, 20-21, and 33-34 of Verplanken as teaching that the indicator includes information on the generated header for the destination address, where headers are generated fro the destination address. (OA2, pg. 4) 7, 25, 43) Applicants note that claims 1, 13, 26, and 29 do not recite "generating an indicator including information on a message", as the Examiner states in para. 7 on pg. 4, and instead recites "generating, for each destination address, at least one indicator including information on the generated header and the at least one descriptor". The cited Verplanken does not teach or suggest the claimed indicator.

The cited col. 7 of Verplanken mentions that a buffer chaining control block (BCCB) which contains information relating to buffer chaining in a message and a message chaining control block (MCCB) containing information relating to the message chaining. An offset field indicates the beginning of the data in the buffer and a message count field gives the number of bytes used in the message.

Although the cited Verplanken discusses information maintained for a message, this does not teach generating an indicator for each destination address having information on a generated header for the destination address. Further, the cited Verplanken does not address the

shortcoming of Hassan which fails to teach that the indicators generated for the destination addresses address the at least one descriptor.

Thus, even if one were to combine the teachings of the different references as the Examiner proposes, the cited combination does not render obvious claims 1, 13, and 29 because the cited combination does not teach or suggest all the claim limitations for which it is recited. Accordingly, claims 1, 13, and 29 are patentable over the cited combination.

Claims 2-12, 14-25, and 30-40 are patentable over the cited art because they depend from one of claims 1, 13, and 29, respectively. Further, the following dependent claims provide additional grounds of patentability over the cited art for the following reasons.

Claims 2, 14, and 30 depend from claims 1, 13, and 29, respectively, and further require that the payload is written to multiple packet entries in the packet memory, wherein one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted

The Examiner cited the above discussed col. 11 as teaching the claim requirement that one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted (OA2, pg. 5) Applicants traverse.

The cited col. 11 mentions that for the MC scheduling operations, leaf index values correspond to N leaf flows associated with a root flow. A linked buffer has an index portion relating to the leaf and root flow index values and a pointer location portion pointing to the cell memory locations, having cells enqueued for an MC service. Hassan mentions that in the MC flow arrangement, a root flow is transmitted to a plurality of egress interfaces using leaf flows, and that a scheduler implements the MC scheduling activity. (Hassan, col. 9, lines 13-25)

Although the cited Hassan discusses a multicast (MC) flow, there is no teaching of the claim requirement that one descriptor is generated for each packet entry including the payload and that one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted. The cited node flows of Hassan do not teach or suggest that there is one indicator for each destination address and descriptor generated for one packet entry.

The cited Verplanken does not address the above discussed deficiencies of Hassan.

Accordingly, claims 2, 14, and 30 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

Claims 6, 18, and 34 depend from claims 1, 13, and 29, respectively, and further require using, for each destination address and indicator associated with the destination address, the information on the generated header in the at least one indicator for the destination address to access the header for the destination address; and transmitting, for each destination address and indicator associated with the destination address, the payload from the entry in the packet memory associated with the indicator and the accessed header for the destination address.

The Examiner cited co. 9, lines 12-16 and FIGs. 1 and 4 of Hassan and col. 7, lines 1-8, 20-21, and 33-34 of Verplanken as teaching the requirements of these claims. (OA2, pg. 9) Applicants traverse.

The cited Hassan mentions a multicast (MC) flow arrangement where a root flow entering an ATM switch is transmitted to a plurality of egress interfaces using corresponding leaf flows. The cited Verplanken mentions a buffer chaining control block (BCCB) which contains information relating to buffer chaining in a message and a message chaining control block (MCCB) containing information relating to the message chaining. An offset field indicates the beginning of the data in the buffer and a message count field gives the number of bytes used in the message.

Nowhere do the cited Hassan and Verplanken teach or suggest that for each destination address and indicator associated with the destination address, information on the header in the indicator is used for the destination address to access the header. The Examiner has not cited where Hassan or Verplanken teach that an indicator associated with a destination address, which addresses a descriptor, is used to access the header for the destination address.

Accordingly, claims 6, 18, and 34 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

Claims 10, 22, and 38 depend from claims 1, 13, and 29, respectively, and further require writing to a local memory at least one handle for each destination address addressing the at least one indicator for the destination address; writing the handles in the local memory to an output

queue; and queuing the indicators corresponding to the handles in the output queue to at least one packet queue.

The Examiner cited col. 8, lines 3-5 and 58-60, col. 12, lines 37-39 and 50-56, and FIGs. 5, 9 of Verplanken as teaching the additional requirements of these claims. (OA2, pg. 14)

The cited col. 8 mentions that free indirect control blocks (ICBs) are gathered in a free indirect control queue and that a DSI may read the address of the next direct control block to a corresponding buffer. The cited col. 12 mentions that in multicast processing, data buffers stored in a data structure in a data store represent a message and that it is not necessary to store the address of the next message, and the directory control blocks may be stored in the CBS and that the indirect control blocks point to the original control block via the MCCB pointer.

Although the cited Verplanken mentions how to store a message, there is no teaching or suggestion of the claim requirement of writing to a local memory a handle for each destination address that addresses an indicator for the destination address, that the handles are queued in an output queue, and that the indicators corresponding to the handles are queued in a packet queue in the output queue. The Examiner has not cited where Verplanken teaches the use of two different queues, one to store handles for each destination address and the other to queue indicators corresponding to the handles in the output queue. Instead, the cited Verplanken mentions buffers and a data structure representing a message. The specific claimed indicators, handles, output queue and packet queue are not taught or suggested in the cited combination.

Accordingly, claims 10, 22, and 38 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

2. Claims 26-28 are Patentable over the Cited Art

The Examiner rejected claims 26-28 as obvious over Hassan in view of Boivie, Verplanken, Tsuchiya and Mamillapalli (U.S. Patent Pub. No. 2005/0111452). Applicants traverse.

Amended claim 26 substantially includes the requirements of amended claims 1, 13, and 29 and additionally recites a switch fabric and a plurality of line cards coupled to the switch fabric, wherein each line card includes a network processor, wherein each network processor

includes a packet memory; and circuitry in communication with the packet memory that performs the operations recited in amended claims 1, 13, and 29.

The Examiner cited the above discussed combination of references with respect to the requirements of claim 26 common to claims 1, 13, and 29. (OA2, pgs. 50-52) Accordingly, claim 26 is patentable over the cited art for the reasons discussed above with respect to claims 1, 13, and 29.

Claims 27 and 28 are patentable over the cited art because they depend from claim 26, which is patentable over the cited art for the reasons discussed below.

Conclusion

For all the above reasons, Applicant submits that the pending claims 1-40 are patentable. Should any additional fees be required beyond those paid, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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